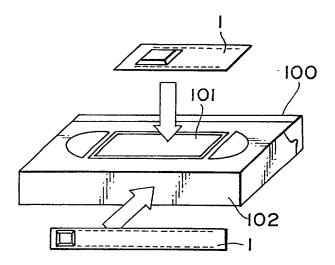
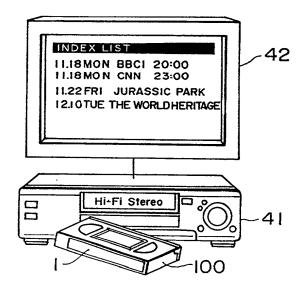
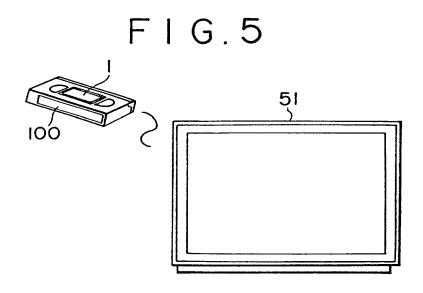


F1G.3



F1G.4





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FIG.6

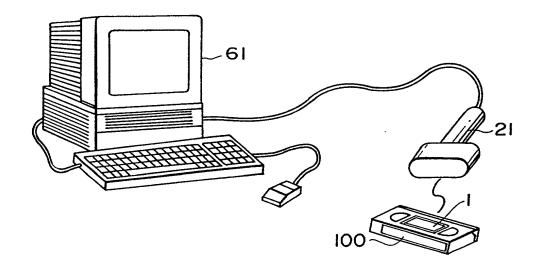


FIG.7

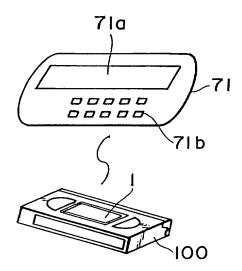
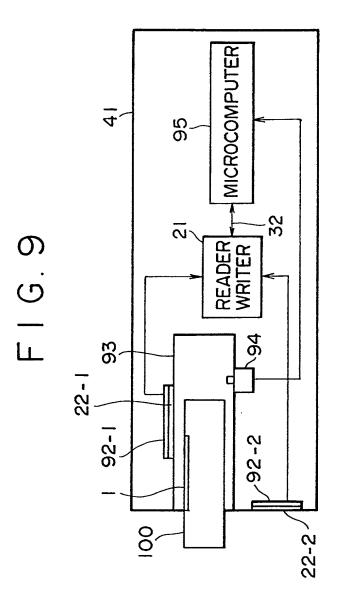


FIG.8
81



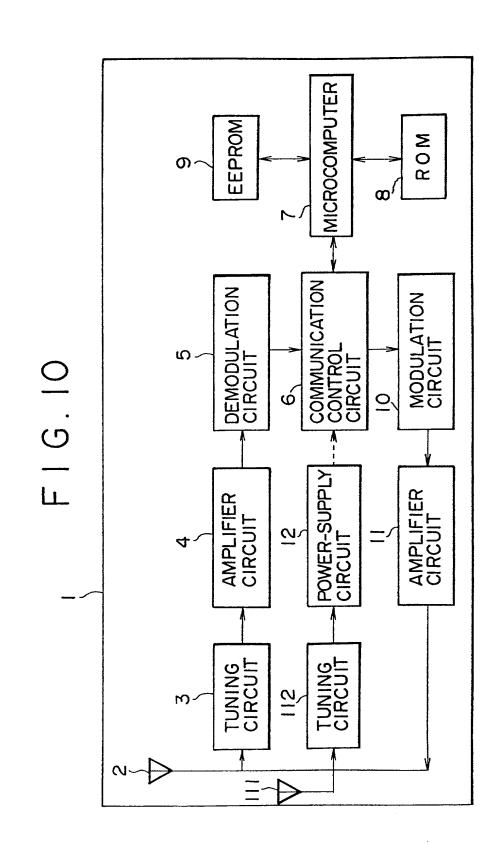
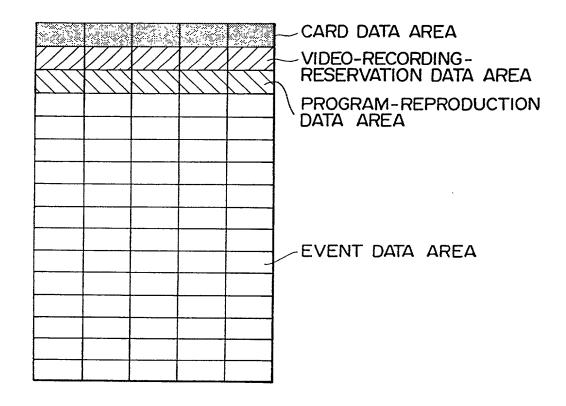
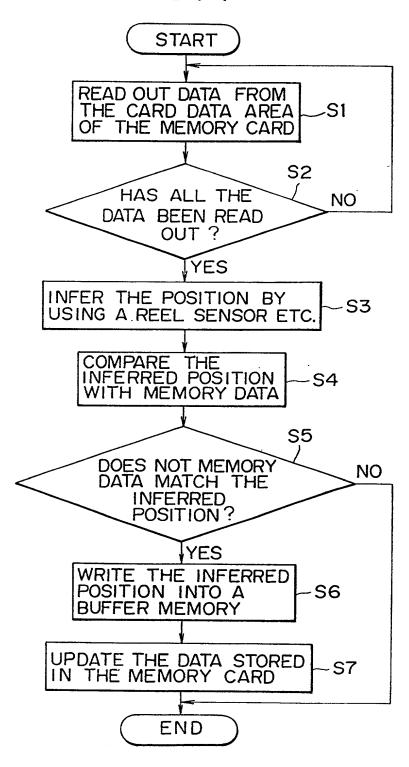


FIG. II



	F	I G) .	12			
MSB						···	LSB
# I Byte	† † #	CAT		1		EVT	
#2Byte				1		МВІ	
#3Byte			T/F			-	U/F
# 4Byte			T/S		1		U/S
#5Byte			T/M	 			U/M
# 6Byte			T/H			1	U/H

FIG.13



F1G.14

	MSB	·		·	.			LSB
# IByte	SR			! !	DAY	(
#2Byte	RP		TCF	T/M			U/M	
#3Byte			T/Y				U/Y	
#4Byte				T/BM				U/BM
#5Byte				T/BH				U/BH
# 6Byte				T/EM	; ; ;		; ;	U/EM
#7Byte		1	; ; ;	T/EH	! ! !			U/EH
#8Byte	 	1	1	ID	† 1 1	1 2 2 4	1	SEL
#9Byte			! !	! ! !	! ! !	1	1 1 1	CHR
# IOByte		1	 	1	1		! !	CHR
# IIByte		!	! ! !	1 1 1] ! !] ! ! !	CHR
# 12Byte		1	1	1	1	1	! ! !	CHR
# I3Byte			1	! ! !	 		1	CHR

F1G.15

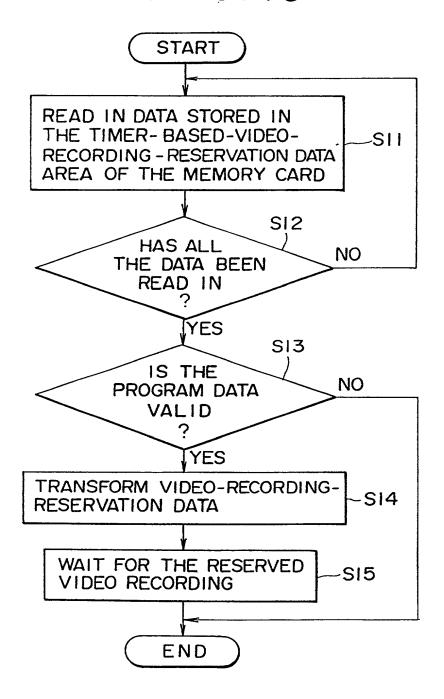
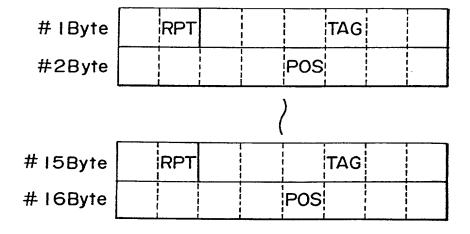
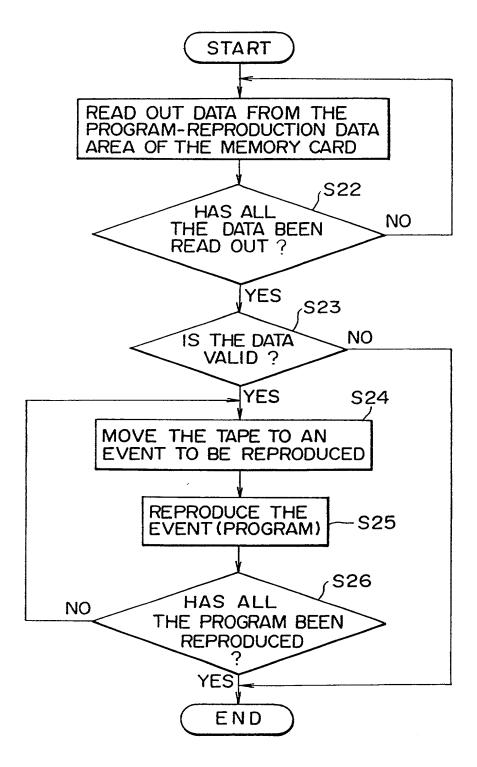


FIG.16



F1G.17

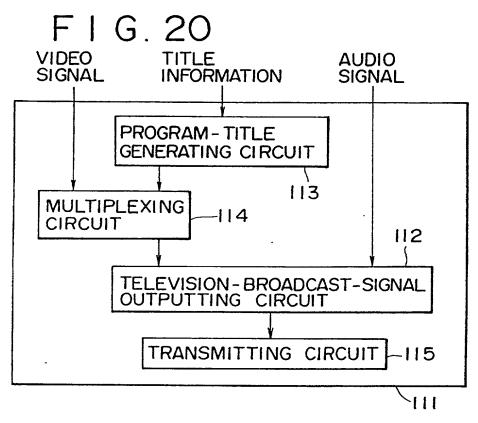


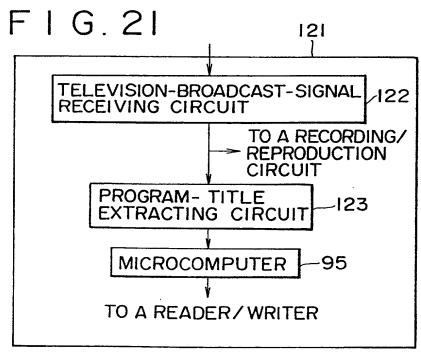
F1G.18

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	MSE	}						LSB	
# I Byte		RM			1	MIN	1		
#2Byte		1	WK		!	HR	 		
#3Byte	MSE	}	YR		 	DAY	1		
#4Byte		! !	YR	LSB		! ! !	МТН		
#5Byte		!	i !	SEL		1	!	ΙD	
#6Byte		! ! !	1	!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!	!	! ! !	! !	CHR	
#7Byte		1	!					CHR	
#8Byte		!	i ! !	1	!	1		CHR	
#9Byte			i !	i ! !	1 1 1			CHR	
# IOByte		: 	 	i i i	• • • • • • • • • • • • • • • • • • •			CHR	
# I I Byte	SR	RP		CHN			AMD		
#12Byte	VEF	AEF	N/C			STY			
# I3Byte			KY1				KYO		
# I4Byte	тхт		вст				CNT		
# I5Byte			ŕ		тсо		! !		
# I6Byte					EBK	i t t			
# I Byte						1	I.	TDP	
#2Byte		i				i		CHR	
)									
ſ		——	-	(<u>1</u>		:		
#32Byte	<u> </u>	1			1	! ! !	! !	CHR	

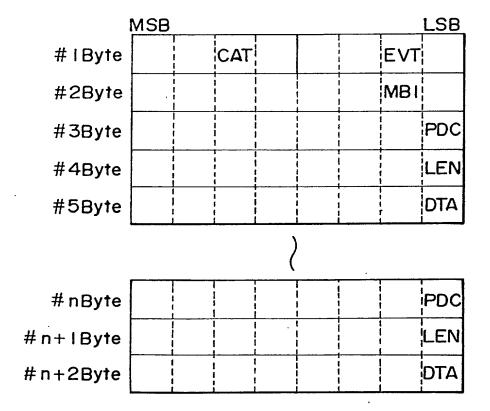
FIG. 19 START READ OUT DATA FROM THE EVENT DATA AREA OF THE MEMORY CARD S31 **S32** HAS ALL NO THE DATA BEEN READ OUT **S33** YES COMPARE THE DATA IN THE MEMORY CARD WITH TEMPORARILY STORED DATA S34 DOES THE DATA MATCH THE NO TEMPORARILY STORED DATA YES WRITE THE TEMPORARILY STORED S35 DATA INTO A BUFFER MEMORY UPDATA THE DATA IN ·S36 THE MEMORY CARD **S37** COMPARE THE DATA IN THE NO MEMORY CARD WITH THE TEMPORARILY STORED DATA FOR VERIFICATION YES END





F I G. 22

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F I G. 23

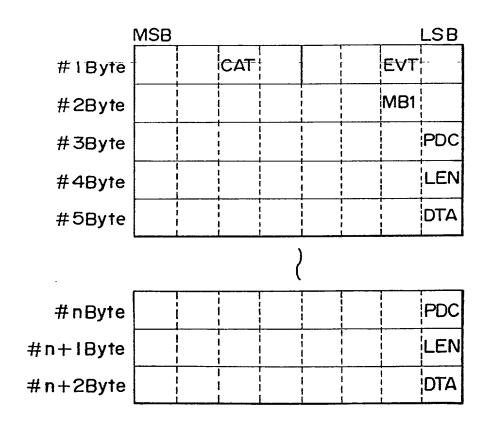
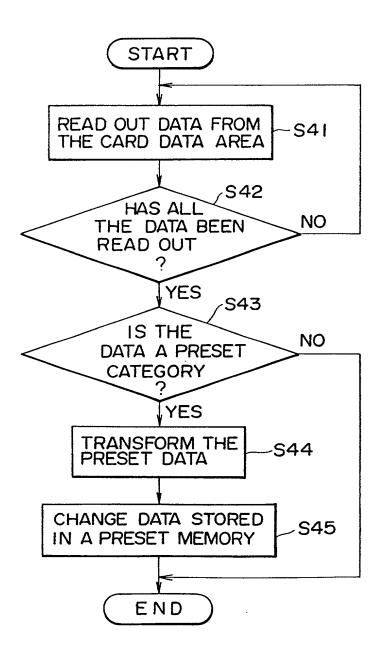
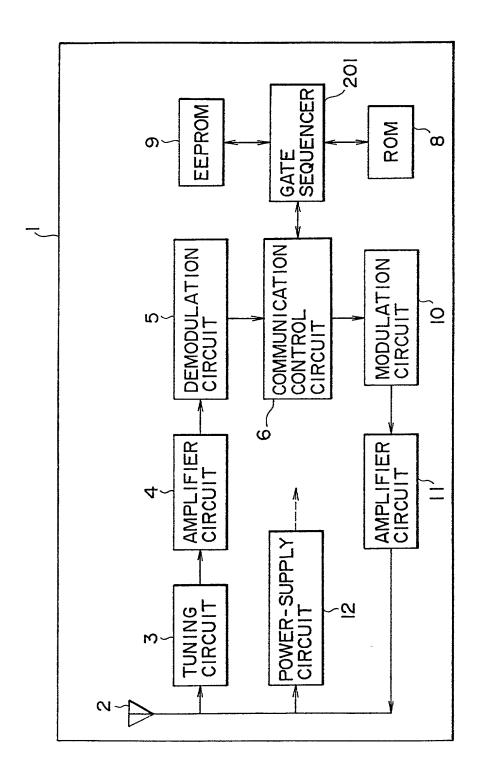


FIG. 24

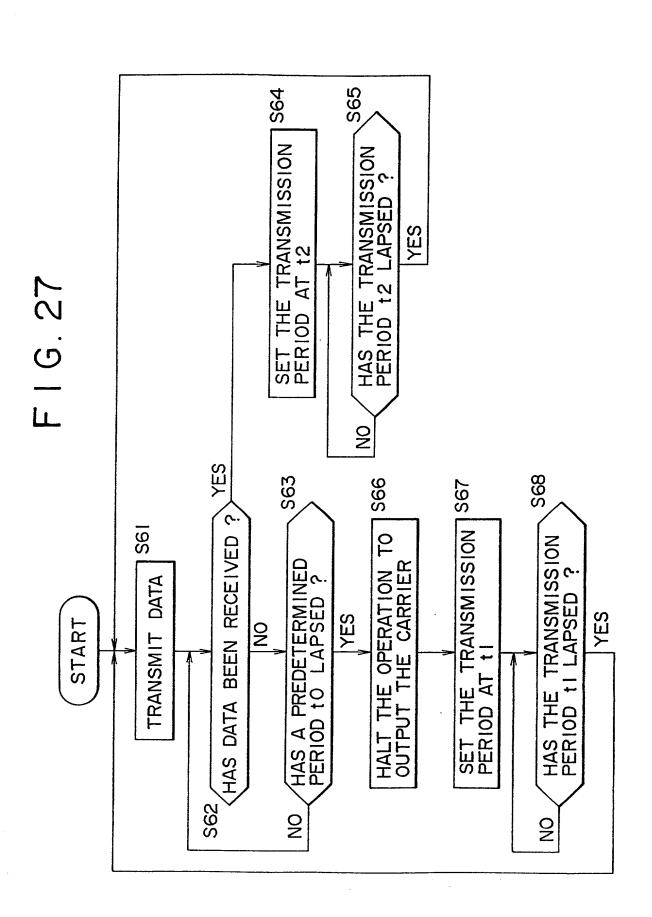


F16.25



EEPROM ത POWER-SUPPLY CIRCUIT | GATE | SEQUENCER | <u>2</u>01 4 <u>2</u>|6 217 215 214 > 213 212 % Σ 232 90 <u>\</u> ~ 23 DEMODULATION CIRCUIT (25

F16.26



F16.28

F16.29

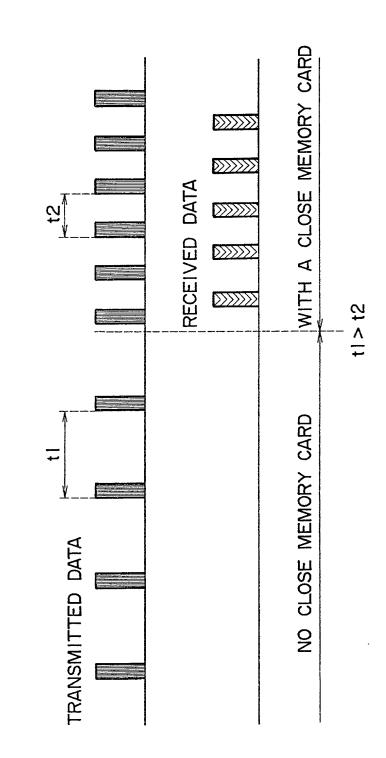
OUTPUT CARRIER TRANSMITTED DATA RECEIVED DATA OUTPUT CARRIER t < t0 TRANSMITTED DATA

RECEIVED DATA

EXAMPLE OF AN OUTPUT CARRIER WITH RECEIVED DATA

EXAMPLE OF AN OUTPUT CARRIER WITH NO RECEIVED DATA

F16.30



F16.31

(i)

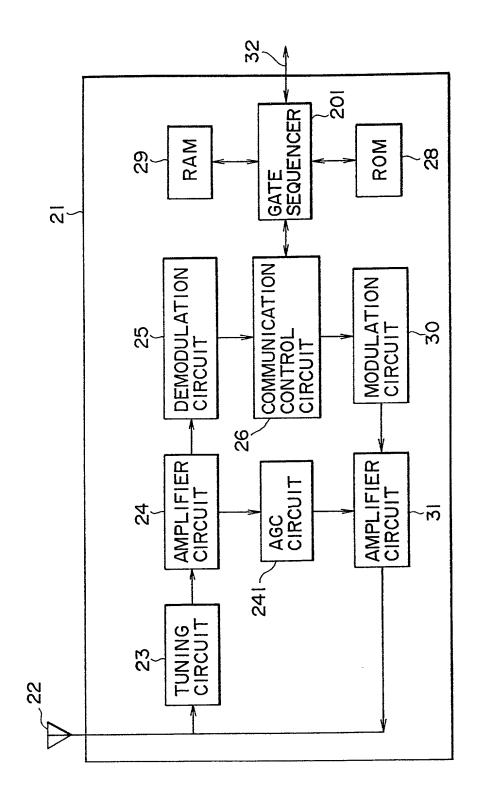
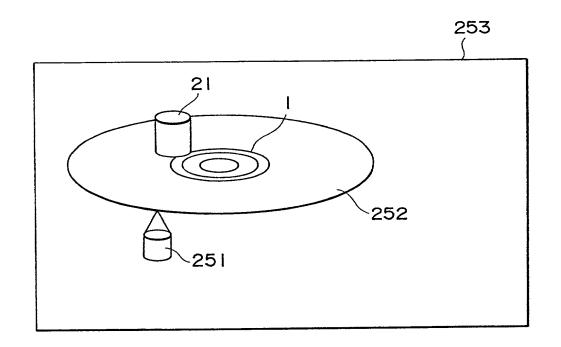


FIG. 32



F I G. 33

